the flatband voltage.

REMARKS

Claims 29-50 are in the application of which claims 29 and 40 are in independent form. Claims 1-28 are cancelled to be replaced by claims 29-50, which more positively recite structural limitations.

An appendix below shows changes to the claims.

Interview. The Examiner is thanked for allowing the inventor Ali Keshavarzi and the undersigned attorney Alan Aldous to have a telephonic interview with the Examiner on September 7, 2001. During the interview, the nature of the rejections in the Office action and the invention were discussed.

IDS. An IDS is being filed to cite Patent 5,962,887 to Manning et al., which was recently cited in a PCT search report. It is believed that the present claims are patentable over it.

Rejections.

Claims 1, 4, 7-14, 17, 20-22, 25, and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (FIG. 1 and FIG. 9).

Claims 2-3, 5-6, 9-13, 15-16, 18-19, 23-24, & 26-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (FIG. 1 and FIG. 9) in view of Chern et al. (US 5,032,892).

The Office action, page 2, states: "Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function." Claims 1-28 have been cancelled and the new claims have been written to positively recite structural limitations.

The new claims are patentable over the admitted prior art (FIG. 1 and FIG. 9) and Chern et al. for at least the following reasons.

First, the claims are patentable over prior art FIGS. 1 and 9 because FIGS. 1 and 9 are in inversion mode and there is no teaching or suggestion in the prior art portion of the present invention to put them in depletion mode.

Second, the claims are patentable over Chern for at least the following reason. Chern is not using the term "depletion mode" in a different sense than is used in the present application. Indeed, the term depletion mode has two different meanings as applied to transistors.

1. Depletion mode vs. enhancement mode

One meaning of depletion mode is to contrast is with enhancement mode transistors. Depletion mode devices are normally on and enhancement devices are normally off. The following explanation comes from G. Rizzoni, Principles and Applications of Electrical Engineering (2nd Ed. 1996), p. 429:

"[The FET of FIG. 8.31] is also called an enhancement-mode device, because the applied field 'enhances' the conduction in the channel by attracting n-type charge carriers. There are also depletion-mode devices, in which the application of an electric field 'depletes' the channel of charge carriers, reducing the effective channel width. It is useful to think of enhancement-mode devices as being normally off: current cannot flow from drain to source unless a gate voltage is applied. On the other hand, depletion-mode devices are normally on; that is, the gate voltage is used to reduce the conduction of current from drain to source." (Emphasis in original.)

Pages 428-439 of G. Rizzoni, Principles and Applications of Electrical Engineering (2nd Ed. 1996) is supplied in an IDS. The undersigned attorney has known of this book for more than three months, but did not know of its significance to the present application until today. Accordingly, it is believed that no IDS late fee is necessary. If the Examiner believes a late fee is necessary, please notify the undersigned attorney.

2. Depletion mode vs. inversion and accumulation modes

Another use of the term "depletion mode" is in contrast to inversion and accumulation modes. This is how the present application uses the term. See, for example, FIG. 2 of the present application.

3. In Chern, depletion mode is in contrast to enhancement mode

In Chern, the depletion mode capacitor is in contrast to an enhancement mode capacitor. See col. 4, line 51 through col. 5, line 28. For example, col. 4, lines 51-59 states:

> "Enhancement mode capacitors require adjustment for their preferential voltage polarity. This can be accomplished through interconnects or similar means. Depletion mode capacitors, on the other hand, have less preferential voltage polarity. If the capacitors are not polarization sensitive, then the capacitors can have a common poly plate 91 or a common active area 95, as schematically shown in FIG. 11."

Chern is directed to engineering capacitors in depletion mode to avoid latch up. Chern does not disclose the polarities of the gate electrode and source/drain diffusions and the voltages to obtain depletion mode in the sense it is used in the present application.

4. Using depletion mode (as opposed to accumulation or inversion modes) in a decoupling capacitor is counter-intuitive and non-obvious

The purpose of a decoupling capacitor is to provide as a high amount of capacitance per unit area of the capacitor. It is counter-intuitive and non-obvious to place a decoupling capacitor in depletion mode because it has less than maximal capacitance. However, as part of the invention of the present invention, the inventors noticed that there is a good tradeoff between leakage and size in depletion mode decoupling capacitors. Accordingly, the claims should be allowed.

Note that merely because applicants do not specifically argue that certain limitations of a claim are not in the references is not a concession that a reference or combination of references includes the limitations. That applicants do not contradict a particular statement made in the Office action is not a concession that applicants agree with it. Further, merely because applicants do not separately argue the patentability of every dependent claim is not a concession that there are not additional reasons for patentability of these dependent claims.

Applicants believe the application is in condition for allowance and respectfully request the same.

Respectfully submitted,

Dated: November 5, 2001

Alan K. Aldous
Reg. No. 31,905

Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1026
Phone: (503) 264-7125
Phone: (503) 684-6200
Phone (310) 207-3800
Facsimile: (503) 684-3245

An appendix with marked up claims begins on the next page.

APPENDIX:

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

Please cancel claims 1-28 and replace them with the follow new claims:

29. A die, comprising:

a first conductor carrying a power supply voltage;

a second conductor carrying a ground voltage; and

a semiconductor decoupling capacitor to provide decoupling capacitance between the first and second conductors, the semiconductor decoupling capacitor including:

(a) a gate electrode coupled to the first conductor to receive the power supply voltage,

(b) a diffusion coupled to the second conductor to receive the ground voltage, and

(c) a body to receive the ground voltage through the diffusion, the semiconductor decoupling capacitor thereby being in depletion mode.

30. The die of claim 29, wherein gate electrode is p-type and the diffusion and the body are n-type.

31. The die of claim 29, wherein gate electrode is p-type and the diffusion and the body are n-type, with the diffusion being more heavily doped than the body.

32. The die of claim 29, wherein the diffusion is a first diffusion and the semiconductor decoupling capacitor further includes a second diffusion coupled to the second conductor to receive the ground voltage and wherein the body receives the ground voltage through the first and second diffusions.

33. The die of claim 32, wherein the first and second diffusions are source/drain diffusions.

34. The die of claim 32, wherein the first and second diffusions are mover heavily doped than the body.

35. The die of claim 29, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.

36. The die of claim 29, wherein gate electrode is p-type and the diffusion and the body are n-type, and wherein the diffusion is a body tap diffusion and the semiconductor decoupling capacitor further includes first and second source/drain diffusions that are p-type.

37. The die of claim 36, wherein the first and second source/drain diffusions are coupled to the second conductor to receive the ground voltage.

38. The die of claim 36, wherein the body tap diffusion and first and second source/drain diffusions are more heavily doped than the body.

39. The die of claim 36, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.

40. (Amended) A die, comprising:

a first conductor carrying a power supply voltage;

a second conductor carrying a ground voltage; and

a semiconductor decoupling capacitor to provide decoupling capacitance between the first and second conductors, the semiconductor decoupling capacitor including:

(a) a gate electrode coupled to the second conductor to receive the ground voltage,

(b) a diffusion coupled to the first conductor to receive the power supply voltage,

(c) a body to receive the power supply voltage through the diffusion, the semiconductor decoupling capacitor thereby being in depletion mode,

(d) a substrate, and

(e) an insulation between the substrate and the body.

41. The die of claim 40, wherein gate electrode is n-type and the diffusion and the body are p-type.

42. The die of claim 40, wherein gate electrode is n-type and the diffusion and the body are p-type, with the diffusion being more heavily doped than the body.

43. The die of claim 40, wherein the diffusion is a first diffusion and the semiconductor decoupling capacitor further includes a second diffusion coupled to the first conductor to receive the power supply voltage and wherein the body receives the power supply voltage through the first and second diffusions.

44. The die of claim 43, wherein the first and second diffusions are source/drain diffusions.

45. The die of claim 43, wherein the first and second diffusions are mover heavily doped than the body.

46. The die of claim 40, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.

47. The die of claim 40, wherein gate electrode is n-type and the diffusion and the body are p-type, and wherein the diffusion is a body tap diffusion and the semiconductor decoupling capacitor further includes first and second source/drain diffusions that are n-type.

48. The die of claim 47, wherein the first and second source/drain diffusions are coupled to the second conductor to receive the ground voltage.

49. The die of claim 47, wherein the body tap diffusion and first and second source/drain diffusions are more heavily doped than the body.

50. The die of claim 47, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.